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(71) Applicant(s)
National Transcommunications Limited

(Incorporated in the United Kingdom)

Crawley Court, WINCHESTER, Hampshire, SO21 2QA, United Kingdom

(72) Inventor(s)
Edwin Loverseed

(74) Agent and/or Address for Service
A A Thornton & Co
Northumberland House, 303-306 High Holborn, LONDON, WC1V 7LE, United Kingdom

(54) Compensating for delays in a multiplexer

(57) A method and apparatus are provided for multiplexing a plurality of data streams for transmission, at least one of the data streams comprising packets of data including clock reference packets. Potential timing problems caused by the multiplexing process altering the timing relationship between packets are avoided by altering the contents of the clock reference packets according to the length of time the packets are held in the multiplex buffer 25. In particular a first count referenced to a local clock counter 27 is subtracted from each program clock reference packet on entry to the buffer, and a second count, also referenced to the local clock counter 27 is added on departure.

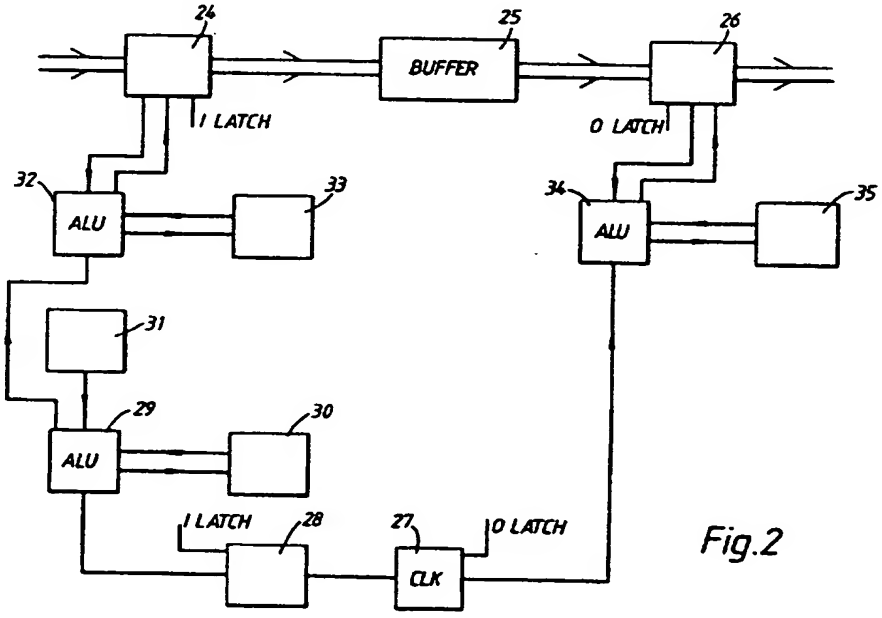

Fig.2

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

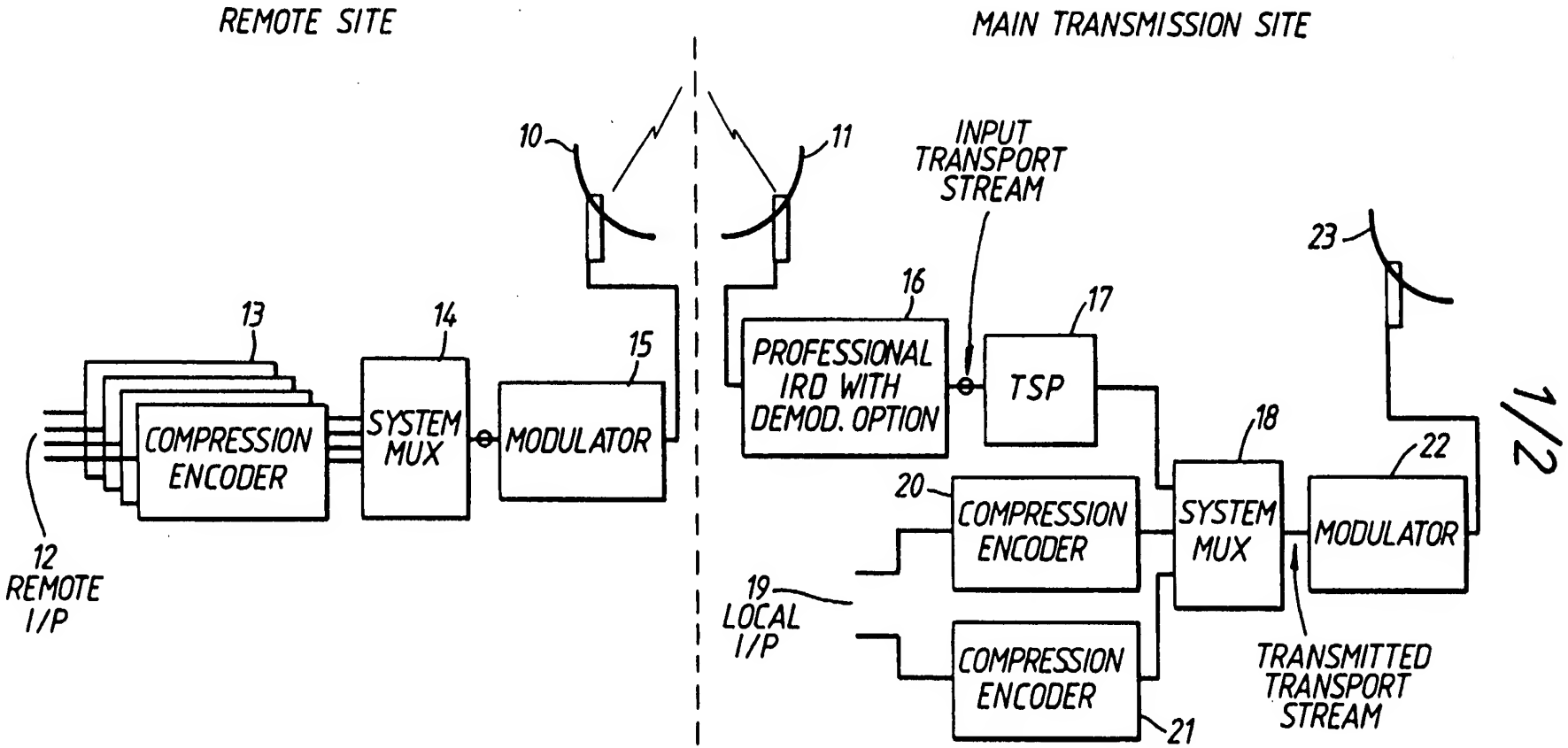

Fig.1

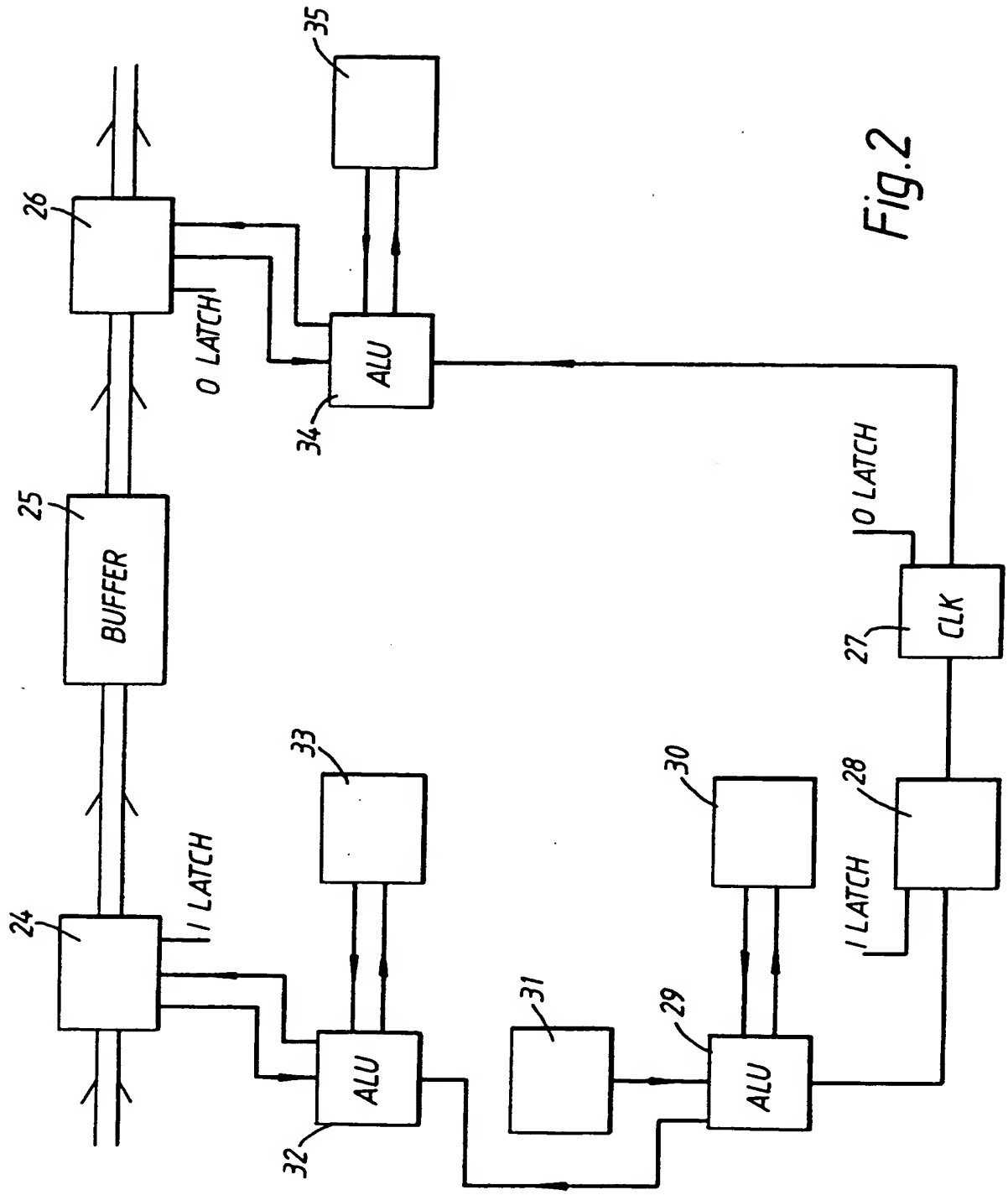

Fig.2

Method and System for Passing Plural Streams of Data through a Multiplexer

The present invention relates to a method and system in which a plurality of streams of digital data are multiplexed for transmission over a single transmission medium. The invention can be applied to data which represents a television or a radio transmission.

It is known to use a multiplexer to multiplex a plurality of streams of asynchronous digital data in which the streams of data are in the form of packets of data, the packets being first stored in one or more transport buffers from which the packets are accessed by the multiplexer. The multiplexer accesses the packets of data at times which are controlled by processing means which form a part of the multiplexer system.

It is also known to include packets within each of the streams of data which consist of program clock reference packets. The program clock reference packets are included in the streams to provide timing information relevant to decoding and resynchronising picture and sound information in the streams of data.

A problem in allowing the multiplexer processing means to determine the timing of access to the packets of data stored in the transport buffers is that the time of access of a program clock reference packet may not correspond to the timing information in the packet. The decoding of the video and audio information by reference to the program clock reference packet would therefore be affected. A need therefore exists to provide a method and system to enable the timing information in the program clock reference packets to be altered in accordance with the timing of access to the program clock reference packets and their onward transmission through the multiplexer.

According to the present invention there is provided a method of passing a plurality of streams of data through a multiplexer for onward transmission over a single transmission medium, at least one of the streams of data comprising an input transport stream of packets of data including program clock reference packets, the method comprising the steps of,

passing the input stream to the multiplexer through a transport stream processor including a transport buffer,

detecting each program clock reference packet in the input transport stream upon entry into the transport buffer,

subtracting from each program clock reference packet, on entry to the transport buffer, a first count referenced to a local clock counter,

detecting each program clock reference packet upon departure from the transport buffer,

and adding to each clock reference packet, upon departure from the transport buffer, a second count value referenced to the local clock counter,

the first and second count values for each program clock reference packet being effective to compensate for the delay imposed on the packet through the transport stream processor.

Further according to the present invention there is provided a system for passing a plurality of streams of data through a multiplexer for onward transmission over a single transmission medium, at least one of the streams of data comprising an input transport stream of packets of data including program clock reference packets, the system comprising,

a transport stream processor including a transport buffer to pass the input transport stream to the multiplexer,

first detecting means to detect each program clock reference packet in the input transport stream on entry to the transport buffer,

a local clock counter,

subtracting means to subtract from each program clock reference packet, on entry to the transport buffer, a first count value referenced to the local clock counter,

second detecting means to detect each program clock reference packet upon departure from the transport buffer,

and adding means to add to each program clock reference packet, upon departure from the transport buffer, a second count value referenced to the local clock counter,

the first and second count values for each program clock reference packet being effective to compensate for the delay imposed on the packet through the transport stream processor.

The invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 is a diagram of a digital television transmission system incorporating the present invention and Figure 2 shows detail of a transport stream processor included in the system of Figure 1.

Referring to Figure 1, there is shown a digital television transmission system including a remote transmission site connected through transmission aerials 10 and 11 to a main transmission site. At the remote site there are provided a plurality of input ports 12 connected through respective compression encoders 13 to a system multiplexer 14 and a modulator 15 to the aerial 10. The input ports each supply a stream of data for encoding and multiplexing by the encoders 13 and multiplexer 14 before modulation by the modulator 15 and onward transmission through the aerials 10 and 11 to the main transmission site as a transport stream of data.

At the main transmission site, the aerial 11 is connected to an integrated receiver/decoder 16 which receives and decodes the data from the aerial 11 and generates therefrom a

transport stream of data. The input transport stream of data is passed through a transport stream processor 17 to be received by a system multiplexer 18. A plurality of local input ports 19, each supply digital television signals in the form of a stream of packets of data to respective compression encoders 20 and 21. The outputs from the compression encoders are supplied to the system multiplexer 18. The output from the system multiplexer is supplied to a modulator 22 for modulation and onward transmission via a single transmission medium through an aerial 23.

It will be apparent that the system multiplexer 18 at the main transmission site is required to receive and multiplex a plurality of streams of digitally encoded data where two of the streams are generated at the main transmission site and one is received from the remote site. The streams of data supplied to the multiplexer 18 consist of packets some of which consist of program clock reference packets which are used to provide clock reference information relevant to decoding asynchronous picture and sound information in the streams of data in a manner which is well known to those skilled in the art. The streams of data are held in transport buffers pending supply to the multiplexer 18 which controls the addressing of the buffered packets of data under the timing of a clock within the system multiplexer 18. The timing of the passage of each individual packet of data through the system multiplexer 18 is therefore controlled by the system multiplexer.

The input transport stream supplied to the transport stream processor 17 has program clock reference packets which are generated remotely from the multiplexer 18 and are therefore outside the control of the multiplexer 18. A problem would arise if the program clock reference packets were to be transmitted through the multiplexer 18 at times which do not correspond to the timing information in the packets because the decoding of the video and audio information by reference

to the program clock reference packets would be adversely affected. The transport stream processor has means to alter the timing information in the clock reference packets of the input transport stream.

Referring now to Figure 2, there is shown the transport stream processor in more detail. The processor 17 includes an input control device 24 to receive the input transport stream of data from the receiver/decoder 16. The input control device 24 is capable of detecting the entry of each program clock reference packet and generates a signal ILATCH in response. From the input control device 24, the input packets of data in the input transport stream are passed to a transport buffer 25 and the packets are subsequently passed to an output control register 26. The output control register 26 is connected to supply packets of data to the system multiplexer 18.

A local reference clock 27 is connected to supply a count value to a latch 28 triggered by the signal ILATCH to register the count value from the clock 27. The latch 28 supplies the registered count value to an arithmetic logic unit 29 which is driven by a driver 30 to subtract a preselected offset value from the count value presented to the unit 29. The offset value is of a magnitude to compensate for the fixed delay suffered by each program clock reference packet during its passage through the transport stream processor and is supplied to the arithmetic logic unit 29 from an offset register 31.

The offset adjusted count value is supplied to a second arithmetic logic unit 32 controlled by a driver 33. The second arithmetic logic unit 32 subtracts the offset adjusted count value from the incoming program clock reference packet. It will thus be appreciated that each program clock reference packet entering the input control register 24 triggers the latch 28 to store the count from

the local reference clock 27. The fixed offset value is then subtracted from the count value in the latch 28. The incoming program clock reference packet has the value in the offset register 31 subtracted before the packet enters the transport buffer 25.

The packets of data in the transport buffer 25 are addressed at times determined by the system multiplexer 18 and passed to the output control register 26. Each program clock reference packet entering the output control register 26 is detected by the output control register 26 which responds by generating an output latch signal OLATCH. The local reference clock responds to the latch signal OLATCH to pass a count value to a third arithmetic logic unit 34 operating under the control of a driver 35. The logic unit 34 acts to add the count value passed thereto from the local reference clock 27 to the program clock reference packet in the output control register 34. The variable and fixed components of the delay suffered by the program clock reference packet in its passage through the transport stream processor are thus compensated by the subtractions performed by the arithmetic logic units 29 and 32 and the addition performed by the third arithmetic logic unit 34.

Whilst the offset value subtracted by the arithmetic logic unit 29 is fixed for a given transport rate of the input transport stream supplied to the transport stream processor, it will be apparent that this value can be programmed to change to another preselected value if the transport rate is altered. The new offset value is fixed in relation to the new transport rate.

While the invention has been described by reference to Figures 1 and 2 which relate to a digital television transmission system, it will be apparent to those skilled in the art that the invention may be applied to the transmission of any multiplexed data and may for example be

applied to a radio transmission system.

CLAIMS

1. A method of passing a plurality of streams of data through a multiplexer for onward transmission over a single transmission medium, at least one of the streams of data comprising an input transport stream of packets of data including program clock reference packets, the method comprising the steps of,

passing the input transport stream to the multiplexer through a transport stream processor including a transport buffer,

detecting each program clock reference packet in the input transport stream upon entry to the transport buffer,

subtracting from each program clock reference packet, on entry to the transport buffer, a first count value referenced to a local clock counter,

detecting each program clock reference packet upon departure from the transport buffer,

and adding to each clock reference packet, upon departure from the transport buffer, a second count value referenced to the local clock counter,

the first and second count values for each program clock reference packet being effective to compensate for the delay imposed on the packet through the transport stream processor.

2. A method as claimed in claim 1, wherein the first count value is a value which is offset by a preselected offset amount from the count in the local clock counter.

3. A system for passing a plurality of streams of data through a multiplexer for onward transmission over a single transmission medium, at least one of the streams of data comprising an input transport stream of packets of data including program clock reference packets, the system comprising,

a transport stream processor including a transport buffer

to pass the input transport stream to the multiplexer,

first detecting means to detect each program clock reference packet in the input transport stream on entry to the transport buffer,

a local clock counter,

subtracting means to subtract from each program clock reference packet, on entry to the transport buffer, a first count value referenced to the local clock counter,

second detecting means to detect each program clock reference packet upon departure from the transport buffer,

and adding means to add to each program clock reference packet, upon departure from the transport buffer, a second count value referenced to the local clock counter,

the first and second count values for each program clock reference packet being effective to compensate for the delay imposed on the packet through the transport stream processor

4. A system as claimed in claim 3, wherein second subtracting means are provided to derive the said first count value by subtracting a preselected offset value from the count in the local clock counter.

The Patent Office

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Application No: GB 9518533.6 **Examiner:** Simon Rees
Claims searched: 1-4 **Date of search:** 29 February 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4M (MTSX1, MTDX1, MTX1, MZ), H4K (KTA), H4P (PPS, PT, PPF)

Int Cl (Ed.6): H04J (3/06), H04L (12/56)

Other: Online: WPI, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP0624983A2	(RCA) Whole document, especially lines 19-26 of column 2, lines 5-21 of column 5, and in particular from line 55 of column 7 to line 17 of column 8.	1 & 3
X,P	WO95/26596A1	(Scientific Atlanta) Whole document, especially lines 13-24 of page 21.	1 & 3

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.